LESSON PLAN

NAME OF FACULTY : Pradeep Singla
DISCIPLINE : ME
SEMESTER : 8th
SUBJECT : Digital Hardware Design
LESSON PLAN DURATION : 15 WEEKS (FROM JANUARY , 2018 TO APRIL, 2018)
WORK LOAD (LECTURE/PRACTICAL)PER WEEK (IN HOURS) :4 LECTURE, 1 Tutorial

WEEK	THEORY	
	Lectrue Day	**Topic (Including Assignment/Test)**
1st	I	Introduction of digital systems & Their importance
	II	Logic gates, K-Map,Boolean Algebra Adders
	III	
	IV	Substractor
2nd	I	BCD Adder code converters
	II	7-segment display,
	III	Designing using multiplexer, demultiplexer,
	IV	
3rd	I	Decoder, encoder.
	II	
	III	Design of two level NAND only and NOR only networks
	IV	Design of multilevel NAND only NOR gate networks.
4th	I	Flip-flop
	II	
	III	Excitation Table and its problems
	IV	FSM
5th	I	
	II	Sequence detector
	III	
	IV	Party checker & Detector and different applicator of sequential ckts
6th	I	
	II	State table state diagram
	III	
	IV	Moore & mealy sequential ckt with state diagram
7th	I	
	II	
	III	Reduction of state table using merger graph method & moore method
	IV	
8th	I	
	II	computing M/C
	III	Limitation & capabilities of seq. Ckt
	IV	FSM, Racer
9th	I	FSM, Racer
	II	State table & flow table diagram
	III	
	IV	
10th	I	compatibility chart state assignment in Asynchronous ckt
	II	
	III	Iterative networks
	IV	
11th	I	Design of parity checker
	II	
	III	Comparator
	IV	design of pattern detector
12th	I	design of pattern detector
	II	state machine design with SM charts
	III	
	IV	
13th	I	state machine charts
	II	Derivation of SM charts
	III	
	IV	Memories: read only memory
14th	I	Memories: read only memory
	II	ROM applications
	III	Read write memories
	IV	Static RAM
15th	I	Dyanmic RAM
	II	Structure and Timings
	III	
	IV	