LESSON PLAN

NAME OF FACULTY : Pradeep Singla
DISCIPLINE : ME
SEMESTER : 8th
SUBJECT : Digital System Design
LESSON PLAN DURATION : 15 WEEKS (FROM JANUARY , 2018 TO APRIL, 2018)
WORK LOAD (LECTURE/PRACTICAL)PER WEEK (IN HOURS) : 4 LECTURE, 2 PRACTICAL, 1 Tutorial

WEEK	THEORY		Practical	
	Lectrue Day	Topic (Including Assignment/Test)	Practical Day	Topic
1st	I	Introduction to digital Systems ans their use in practical life	Ist	Introduction to demonstrate and understand the VHDL.
	II	Overview to entire syllabus		
	III	Design for Testability		
	IV	Design for Testability		
2nd	I	Estimating Digital System Reliability	2nd	Write a VHDL script to understand the basic gate realization.
	II			
	III	Transmission lines		
	IV	Reflections and Transmissions		
3rd	I	Timing hazards, Static hazards using Maps	3rd	Write a VHDL script to understand the more gate realization using behavioral modeling.
	II			
	III	Dynamic hazards, Designing hazards free circuits		
	IV			
4th	I	Barrel shifter design	4th	Write a VHDL script to understand the gates realization using structural modeling.
	II	Simple Floating point encoder		
	III	**Unit-I Test**		
	IV	Introduction to state Machines		
5th	I	Clocked Synchronous state Machine Design	5th	Write a VHDL script to understand the gates realization using dataflow modeling.
	II	Designing state machine using state diagram		
	III			
	IV	State machine synthesis using transition lists		
6th	I	State machine design examples	6th	Write a VHDL script to design the adders.
	II			
	III	Decomposing State machine		
	IV			
7th	I	Feedback Sequential Circuits	7th	Write a VHDL script to design the subtractor.
	II			
	III	Feedback Sequential Circuit design		
	IV			
8th	I	Unit-2 Test	8th	Write a VHDL script to design the multiplexer and demultiplexer
	II	Synchronous system structure		
	III			
	IV	Impediment to Synchronous Design		
9th	I		9th	Write a VHDL script to design the encoder and decoder.
	II	Synchronizer failure		
	III			
	IV	Meta-stability		
10th	I		10th	Write a VHDL script to design the flip-flops.
	II	Introduction of Finite State Machine		
	III	Describe the sequential behavior using a FSM, Example of FSM		
	IV			
11th	I		11th	Write a VHDL script to design the registers and counters.
	II	Convert a finite state machine to a Controller		
	III			
	IV	Sequential circuit having a register and combinational logic		
12th	I		12th	Write a VHDL script to design the Finite State Machine.
	II			
	III	Analytical modeling of Moore and Mealy machine		
	IV			
13th	I			
	II			
	III			
	IV	Introducing Key Symbols used in PLD Design		
14th	I			
	II	Programmable Read Only Memory (PROM)		
	III	Programmable Logic Arrays (PLA),		
	IV	Programmable Array Logic (PAL)		
15th	I	Generic Array Logic (GAL).		
	II	Practice/Revision Session		
	III			
	IV			